**Digital Design and Computer Organization Laboratory**

**3rd Semester, Academic Year 2024**

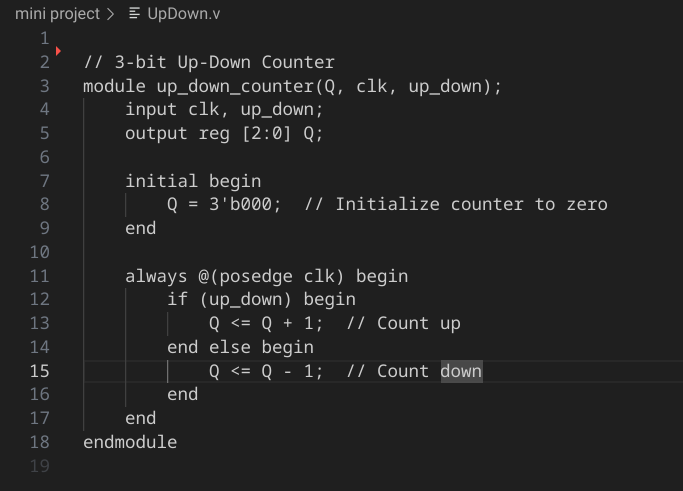
Date: 20/10/2024

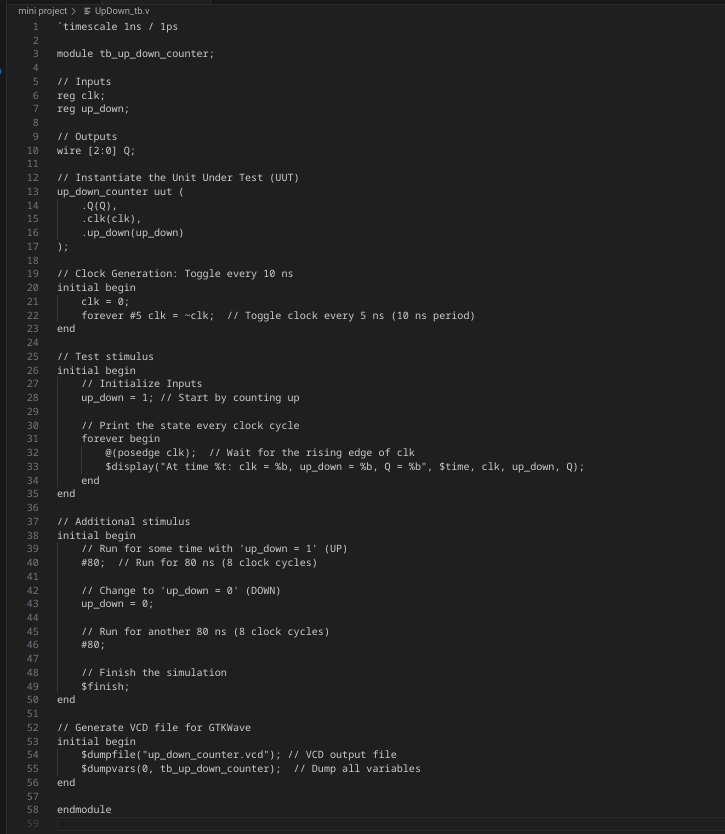
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| Team members: Rithvik Rajesh Matta  Rishi A Sheth  Rohan  Ritesh M | SRN: PES2UG23CS485  PES2UG23CS479  PES2UG23CS489  PES2UG23CS483 | Section: H |

Aim of the Experiment:

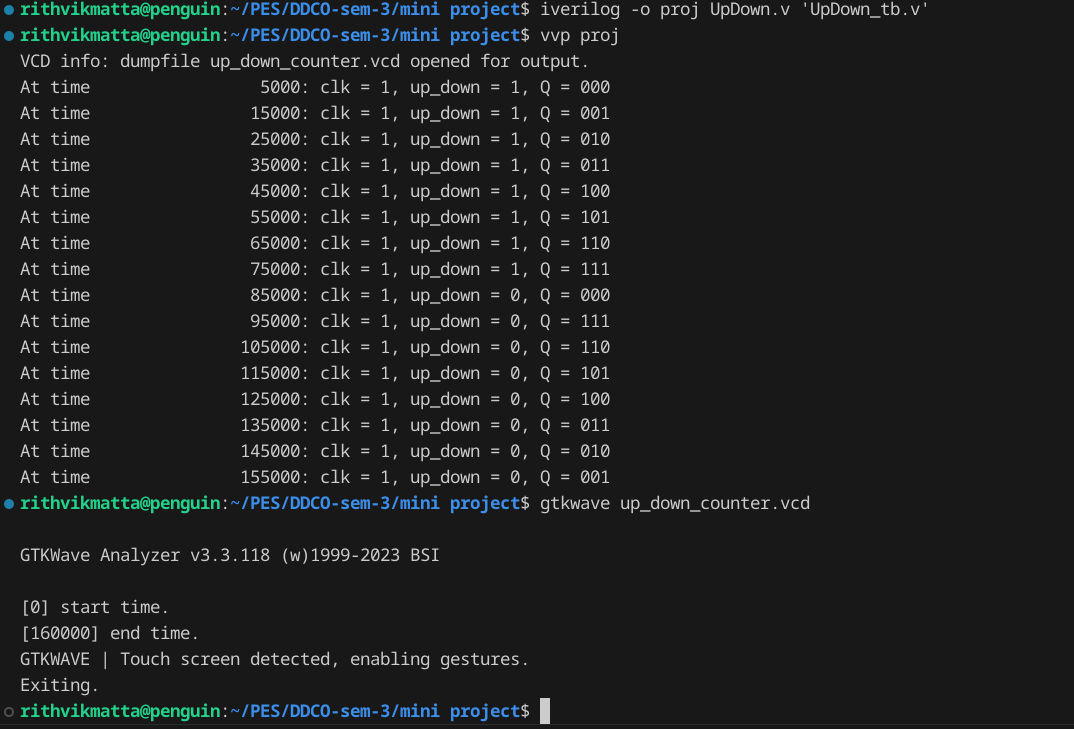
TO DESIGN AND IMPLEMENT A 3-BIT UP/DOWN COUNTER THAT INCREMENTS OR DECREMENTS ITS COUNT VALUE BASED ON CONTROL SIGNALS, FOLLOWED BY GENERATING THE VERILOG VVP OUTPUT AND SIMULATION WAVEFORM USING GTK WAVE, AND VERIFYING THE OUTPUT AND WAVEFORM AGAINST THE TRUTH TABLE.

I. Verilog Code Screenshot

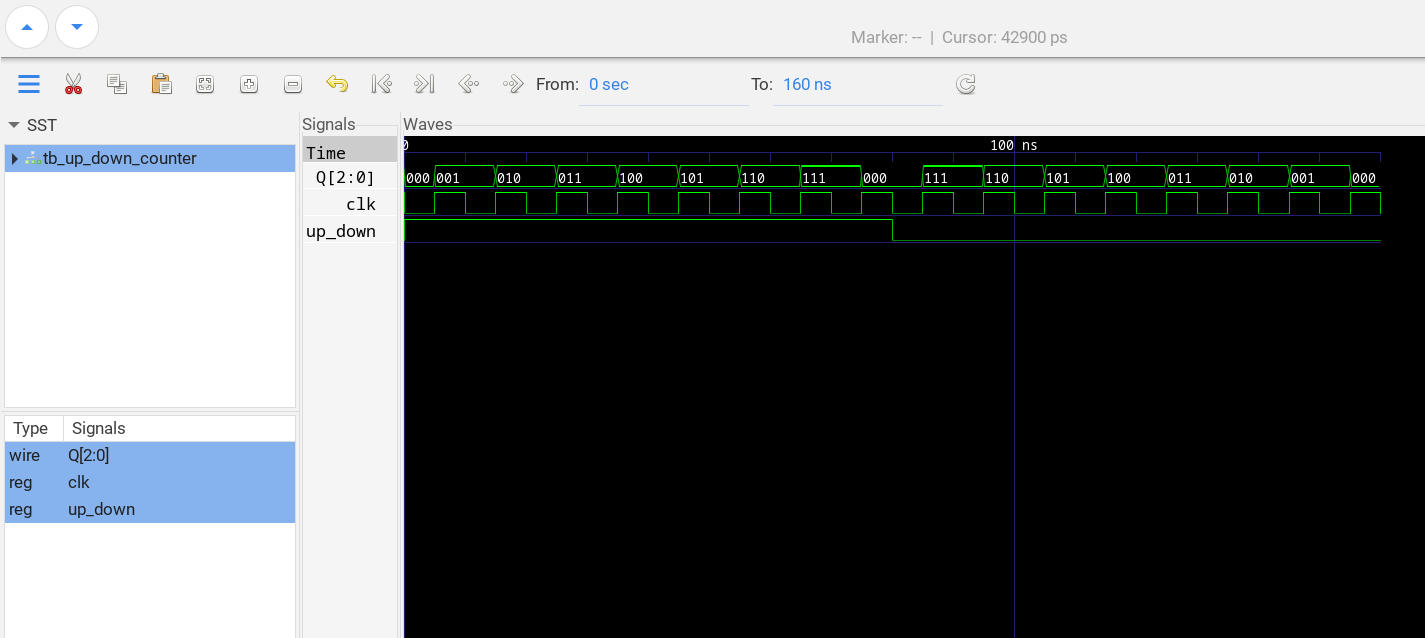




II. Verilog VVP Output Screen Shot



III. GTKWAVE Screenshot



IV. Output Table (Truth Table)

|  |  |  |  |
| --- | --- | --- | --- |
| **M** | **Q3** | **Q2** | **Q1** |

Up counter

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 |

Down counter

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |